REMARKS

In the last Office Action, the Examiner rejected claims 1-3 and 33 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,361,685 to Tanaka in view of U.S. Patent No. 6,130,311 to Kurz et al. ("Kurz") and U.S. Patent No. 6,152,970 to Wei et al. ("Wei"). Claims 1-11 and 33-55 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,247,277 to Mori et al. ("Mori") or U.S. Patent No. 6,489,062 to Watanabe et al. ("Watanabe") in view of Wei.

In accordance with the present response, independent claim 4 has been amended to further patentably distinguish from the prior art of record by incorporating the subject matter of claims 5 and 35. More specifically, independent claim 4 has been amended to recite the step of welding an outer connection terminal to the heated assembled coin- or button-type electrical double layer capacitor (claim 5) and that a temperature profile of the reflow soldering step is approximately the same as a temperature profile of the heating step (claim 35). Claim 4 has been further amended to recite that the heated assembled coin- or button-type electrical double layer capacitor is reflow soldered on the circuit substrate using the outer connection terminal.

Independent claim 1 has been amended to further patentably distinguish from the prior art of record by incorporating the subject matter of claim 2 directed to the welding of an outer connection terminal, and further in a manner similar to claim 4 by reciting that a temperature profile of the heating step is approximately the same as a temperature profile of reflow soldering.

Independent claims 36 and 43 have also been amended to further patentably distinguish from the prior art of record by incorporating the subject matter of claims 37, 39-40 and 44, 46-47, respectively. Claims 36 and 43 have also been amended in a manner similar to claims 1 and 4, respectively, to recite that a temperature profile of the heating step is approximately the same as a temperature profile of reflow soldering (claim 36) and that a temperature profile of the reflow soldering step is approximately the same as a temperature profile of the heating step (claim 43). Claim 43 has been further amended to recite that the heated assembled coin- or button-type electrical double layer capacitor is reflow soldered on the circuit substrate using the connection terminal. Claim 55 has been amended to correctly depend on claim 43 rather than claim 42. Claims 2, 5-11, 37, 39-40, 44, 46-47 and 49-54 have been canceled. The previously submitted abstract has been amended to more clearly reflect the invention to which the amended and new claims are directed.

The amendments to the claims made herein do not raise new issues requiring further search and/or consideration. Instead, independent claims 1, 4, 36 and 43 have been amended to further patentably distinguish from the prior art of record by incorporating the subject matter of claims 2, 5, 35, 37, 49-40 and 44, 46-47, respectively, and by defining with more particularity the relationship of the temperature profile of the heating step to a temperature profile of reflow soldering (claims 1, 36), the relationship of the temperature profile of the heating step to the temperature profile of the reflow soldering step (claim 43), and the use of an outer connection terminal (claim 4) or a connection terminal (claim 43) to reflow solder the heated assembled coin- or button-type electrical double layer capacitor on the circuit substrate, claim 55 has been amended to correctly depend on claim 43, and claims 2, 5-11, 37, 39-40, 44, 46-47 and 49-54 have been canceled, thereby placing the application in condition for allowance or otherwise substantially reducing the issues which remain for appeal.

Applicants respectfully request reconsideration of their application in light of the following discussion.

Brief Summary of the Invention

The present invention is directed to a method of producing an electrical double layer capacitor and to a method of mounting the electrical double layer capacitor on a circuit substrate.

Conventional coin- or button-type electrical double layer capacitors which are mounted on a circuit board by reflow soldering utilize an organic solvent for the electrolyte, a metallic oxide for the positive electrode, and a negative electrode containing lithium to provide the active material. In such conventional capacitors, the components are active by nature. Accordingly, if the quantity ratio of the components changes depending on the fluctuation in the production process, such a change could cause bulging and/or liquid leakage (e.g., leaking of the electrolyte to the outside of the capacitors) during reflow soldering when the capacitors are mounted on the circuit board.

Furthermore, the adequate performance of electrical double layer capacitors mounted by reflow soldering must be assured after reflow soldering. However, there are some cases in which the capacitors contain a large amount of foreign substances (e.g., water). At room temperature, the characteristics of such capacitors are not influenced. However, after reflow soldering or after storage of such

capacitors, a sudden deterioration occurs in the characteristics of such capacitors.

The present invention overcomes the drawbacks of the conventional art. Figs. 1-2 show an embodiment of an electrical double layer capacitor produced by the method according to the present invention embodied in amended independent claim 1. A positive electrode 101, a negative electrode 104, a non-aqueous solvent 102, an electrolyte 109 containing a supporting salt, a separator 108, and a gasket 107 are assembled together to form a coin- or button-type electrical double layer capacitor. The assembled coin- or button-type electrical double layer capacitor is then heated so that a temperature profile of the heating step is approximately the same as a temperature profile of reflow soldering. An outer connection terminal is then welded to the heated assembled coin- or button-type electrical double layer capacitor.

In another aspect, the present invention is directed to a method of mounting an electrical double layer capacitor on a circuit substrate. With reference to Fig. 1, a positive electrode 101, a negative electrode 104, a non-aqueous solvent 102, an electrolyte 109 containing a supporting salt, a separator 108, and a gasket 107 are assembled together to form a coin- or button-type electrical double layer capacitor. The

assembled electrical double layer capacitor is then heated and an outer connection terminal is welded to the heated assembled coin- or button-type electrical double layer capacitor. Thereafter, the heated assembled electrical double layer capacitor is arranged on a circuit substrate and reflow soldered using the outer connection terminal. A temperature profile of the reflow soldering step is approximately the same as a temperature profile of the heating step.

By the foregoing methods according to the present invention embodied in the claims, foreign substances (e.g., water) contained in the assembled electrical double layer capacitor are removed during the heating step which is conducted prior reflow soldering. Additionally, bulging and liquid leakage (e.g., leaking of the electrolyte to the outside of the capacitor) during reflow soldering are prevented when the capacitor is mounted on the circuit board.

The prior art of record does not disclose or suggest the subject matter recited in the pending amended claims.

Traversal of Prior Art Rejections

Claims 1, 3 and 33 were rejected under 35 U.S.C. §103(a) as being unpatentable over Tanaka in view of Kurz and further in view of Wei. Applicants respectfully traverse this rejection and submit that the combined teachings of Tanaka,

Kurz and Wei do not disclose or suggest the subject matter recited in amended claims 1, 3 and 33.

Amended independent claim 1 is directed to a method for producing an electrical double layer capacitor and requires the steps of assembling together components comprised of a positive electrode, a negative electrode, a non-aqueous solvent, an electrolyte containing a supporting salt, a separator, and a gasket to form a coin- or button-type electrical double layer capacitor, heating the assembled coin- or button-type electrical double layer capacitor so that a temperature profile of the heating step is approximately the same as a temperature profile of reflow soldering, and welding an outer connection terminal to the heated assembled coin- or button-type electrical double layer capacitor. No corresponding combination of steps are disclosed or suggested by the prior art of record.

The primary reference to Tanaka discloses a method in which a positive electrode, a negative electrode, and a non-aqueous electrolyte are assembled together to form a non-aqueous battery. As recognized by the Examiner, Tanaka does not disclose or suggest the assembly of an electrical double layer capacitor and the steps of heating the assembled double layer capacitor and welding an outer connection terminal to the heated assembled coin- or button-type electrical double

layer capacitor, as required by independent claim 1. Likewise, Tanaka does not disclose or suggest that a temperature profile of the heating step is approximately the same as a temperature profile of reflow soldering, as required by amended independent claim 1.

The Examiner cited the secondary reference to Kurz for its disclosure of polyester films used to produce film capacitors. In Kurz, the polyester films are heat-treated for the purpose of ensuring the heat stability of the polyester films and the soldering-bath stability of the resulting capacitors (col. 1, lines 25-29). However, Kurz does not disclose or suggest a step of heating a capacitor after the capacitor has been assembled (e.g., assembled using the polyester films), as required by amended independent claim 1. Contrary to the Examiner's contention, in Kurz the heating step during fabrication of the capacitor corresponds to heat-treatment of the polyester films (see examples and comparative examples in columns 5-6), not to a step of heating the capacitor after it has been assembled. Furthermore, Kurtz clearly does not disclose or suggest that a temperature profile of the heating step is approximately the same as a temperature profile of reflow soldering, as required by amended independent claim 1.

The secondary reference to Wei has been cited by the Examiner for presumably disclosing that batteries and capacitors have similar characteristics. However, Wei does not disclose or suggest a step of heating a capacitor after the capacitor has been assembled and that a temperature profile of the heating step is approximately the same as a temperature profile of reflow soldering, as required by amended independent claim 1.

Since Kurz and Wei do not disclose or suggest the foregoing steps recited in independent claim 1, they do not cure the deficiencies of Tanaka. Accordingly, one ordinarily skilled in the art would not have been led to modify the references to attain the claimed subject matter.

Moreover, while acknowledging that the combined teachings of Tanaka, Kurtz and Wei do not disclose the step of welding an outer connection terminal to the heated assembled coin- or button-type electrical double layer capacitor, the Examiner contends that "it is a common practice in the art to weld the capacitor to external terminals allowing connection of the capacitor with the controlling circuitry of an instrument." Applicants respectfully disagree with the Examiner's contention.

In order to support a claim rejection based upon obviousness under 35 U.S.C. §103, the Examiner must provide an

evidentiary basis establishing the obviousness of each modification. The Examiner may do this by citing a reference which directly establishes this obviousness, or, the Examiner may otherwise set forth a line of reasoning consistent with and motivated by the cited art establishing that such modifications would have been obvious. Mere speculation or conclusory allegations are simply inadequate to meet this burden. There must be some teaching, reason, suggestion, or motivation found in the prior art references to make a combination which renders an invention obvious within the meaning of 35 U.S.C §103. See, e.g., Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 982, 989, 18 USPQ2d 1885 (Fed. Cir. 1991).

In order to set forth a prima facie case of obviousness, the Examiner must not only demonstrate that this teaching exists in the prior art, but that it would teach all limitations of the claim. This burden cannot be met by citing references that, even if combined, fail to teach explicitly recited limitations.

Stated otherwise, in rejecting a claim as obvious under 35 U.S.C. §103, the Examiner cannot simply rely on a combination of references that teach some limitations of the claim, and make mere conclusory allegations that the combination teaches others as well.

In the instant case, the Examiner has not met his burden of establishing a prima facie case of obviousness as discussed above.

As noted by the Court of Appeals for the Federal Circuit in the case of In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992):

> 'Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under section 103, teachings of references can be combined only if there is some suggestion or incentive to do so.' Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious 'modification' of the prior art. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. Wilson and Hendrix fail to suggest any motivation for, or desirability of, the changes espoused by the Examiner and endorsed by the Board.
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> Here, the Examiner relied upon hindsight to arrive at the determination of obviousness. It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that '[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.'

As further noted by the Federal Circuit in In re Oeticker, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992):

> The prima facie case is a procedural tool of patent examination, allocating the burdens of going forward as between examiner and applicant. In re Spada, 911 F.2d 705, 707 n.3, 15 USPQ2d 1655, 1657 n.3 (Fed. Cir. 1990). The term 'prima facie case' refers only to the initial examination step. In re Piasecki, 745 F.2d1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976). As discussed in In re Piasecki, the examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a prima facie case of unpatentability. If that burden is met, the burden of coming forward with evidence or argument shifts to the applicant.
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> If examination at the initial stage does not produce a prima facie case of unpatentability, then without more the applicant is entitled to grant of the patent. See In re Grabiak, 769, F.2d 729, 733, 226 USPQ 870, 873 (Fed. Cir. 1985); In re Rinehart, supra.
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> In reviewing the examiner's decision on appeal, the Board must necessarily weigh all of the evidence and argument. An observation by the Board that the examiner made a prima facie case is not improper, as long as the ultimate determination of patentability is make on the entire record. In re Piasecki, 745 F.2d at 1472, 223 USPQ at 788; In re Rinehart, 531 F.2d at 1052, 189 USPQ at 147.

The Federal Circuit has therefore made it clear that the prior art must show an incentive to modify its teachings in order to render a claim obvious. Without such an incentive, a prima facie case of obviousness cannot be made.

Similarly, as the Board stated in Ex Parte Clapp, 227 USPQ 972, 973 (BPAI 1985):

> To support the conclusion that the claimed combination is directed to obvious subject matter, either the references must expressly or impliedly expound the modifications urged by the examiner to have been obvious.

The same situation exists here. The Examiner has not provided an evidentiary basis establishing the obviousness of his proposed modification of Tanaka to provide a step of welding an outer connection terminal to the heated assembled coin- or button-type electrical double layer capacitor, as required by independent claim 1. There is nothing in the references to Tanaka, Kurtz and Wei that would expressly or implicitly teach or suggest the modification urged by the Examiner and, therefore, the references do not directly establish this obviousness. Furthermore, the Examiner has not set forth a line of reasoning consistent with and motivated by the cited art establishing that such modification would have been obvious. The only basis for the modification urged by the Examiner in the rejection is applicants' own disclosure,

and such hindsighted rejections are improper. See, for example, Diversitech Corp. v. Century Steps, Inc., 7 USPQ2d 1315, 1318 (Fed. Cir. 1988); In re Geiger, 2 USPQ2d 1276, 1278 (Fed. Cir. 1987); Panduit Corp. v. Dennison Manufacturing Co., 227 USPQ 337, 343 (Fed. Cir. 1985); Interconnect Planning Corp. v. Feil, 227 USPQ 543, 551 (Fed. Cir. 1985).

Claims 3 and 33 depend on and contain all of the limitations of amended independent claim 1 and, therefore, distinguish from the references at least in the same manner as claim 1.

In view of the foregoing, applicants respectfully request that the rejection of claims 1, 3 and 33 under 35 U.S.C. §103(a) as being unpatentable over Tanaka in view of Kurz and Wei be withdrawn.

Claims 1, 3, 4, 33-36, 38, 41-43, 45, 48 and 55 were rejected under 35 U.S.C. §103(a) as being unpatentable over Mori or Watanabe in view of Wei. Applicants respectfully traverse this rejection and submit that the combined teachings of Mori or Watanabe and Wei do not disclose or suggest the subject matter recited in the amended claims.

Amended independent claim 1 is directed to a method for producing an electrical double layer capacitor as set forth above for the rejection of claims 1, 3 and 33 under 35 U.S.C. §103(a).

Amended independent claim 36 is also directed to a method for producing an electrical double layer capacitor and requires the step of heating the assembled electrical double layer capacitor to remove at least a substantial amount of the foreign substance contained in the assembled electrical double layer capacitor and that a temperature profile of the heating step is approximately the same as a temperature profile of reflow soldering.

Amended independent claims 4 and 43 are directed to a method of mounting an electrical double layer capacitor on a circuit substrate. Claim 4 requires the steps of heating the assembled electrical double layer capacitor and reflow soldering the heated assembled electrical double layer capacitor on the circuit substrate, and that a temperature profile of the reflow soldering step is approximately the same as a temperature profile of the heating step. Claim 43 requires the steps of heating the assembled electrical double layer capacitor to remove at least a substantial amount of the foreign substance contained in the assembled electrical double layer capacitor and reflow soldering the heated assembled electrical double layer capacitor on the circuit substrate, and that a temperature profile of the reflow soldering step is approximately the same as a temperature profile of the heating step.

Applicants respectfully submit that the combined teachings of the references do not disclose or suggest the combination of steps recited in amended independent claims 1, 4, 36 and 43.

The primary reference to Mori discloses an organic electrolyte battery which is caused to pass a high frequency reflow furnace to perform a reflow furnace passage resistance test. The primary reference to Watanabe discloses a non-aqueous electrolyte secondary battery capable of withstanding a reflow temperature. While acknowledging that Mori and Watanabe do not disclose forming an electrical double layer capacitor, the Examiner contends that such step is rendered obvious by the secondary reference to Wei which presumably discloses that batteries and double layer capacitors are formed in a similar manner and have similar characteristics. Applicants respectfully disagree with the Examiner's contention.

It is unclear how the specific disclosure in Wei cited by the Examiner relates to batteries and double layer capacitors having similar construction and/or characteristics. Nevertheless, even if Wei is interpreted to contain such disclosure, Wei does not suggest the modifications that would be needed to replicate the claimed invention. More specifically, none of the cited references discloses or

suggests the combination of steps for producing the electrical double layer capacitor (claims 1, 36) or the combination of steps for mounting the electric double layer capacitor on a circuit substrate (claims 4, 43), as required by amended independent claims 1, 4, 36 and 43.

First, each of amended independent claims 1, 4, 36 and 43 requires the step of forming a double layer capacitor of the coin- or button-type. This step is not disclosed by any of the cited references which disclose the construction of a battery.

Second, each of amended independent claims 1 and 36 requires that a temperature profile of the heating step is approximately the same as a temperature profile of reflow soldering. Likewise, each of amended independent claims 4 and 43 requires that a temperature profile of the reflow soldering step being approximately the same as a temperature profile of the heating step. While disclosing reflow temperature characteristics of particular batteries, Mori and Watanabe do not disclose or suggest the specific relationship between the temperature profiles of the heating and reflow soldering steps. Furthermore, the cited references do not disclose or suggest the step of heating an assembled coin- or button-type double layer capacitor, as required by each of independent claims 1, 4, 36 and 43.

Thus amended independent claims 1, 4, 36 and 43 are not rendered obvious by Mori or Watanabe, as modified by Wei, because the references do not suggest the modifications that would be needed to replicate the claimed invention. In the context of obviousness rejections based upon the purported obviousness of effecting a required modification, the Federal Circuit has held that "[t]he mere fact that the prior art may be modified in [a given] manner ... does not make the modification obvious unless the prior art suggested the desirability of the modification". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992). There is nothing in the cited references that would have suggested the method of forming a coin- or button-type electrical double layer capacitor having the foregoing characteristics recited in amended independent claims 1, 4, 36 and 43.

Claims 3, 33, 34, 35, 38, 41, 42 and 45, 48, 55 depend on and contain all of the limitations of amended independent claims 1, 4, 36 and 43, respectively, and, therefore, distinguish from the references at least in the same manner as claims 1, 4, 36 and 43.

In view of the foregoing, applicants respectfully request that the rejection of claims 1-11 and 33-55 under 35 U.S.C. §103(a) as being unpatentable over Mori or Watanabe in view of Wei be withdrawn.

The amendments to the claims made herein do not raise new issues requiring further search and/or consideration. Instead, independent claims 1, 4, 36 and 43 have been amended to further patentably distinguish from the prior art of record by incorporating the subject matter of claims 2, 5, 35, 37, 49-40 and 44, 46-47, respectively, and by defining with more particularity the relationship of the temperature profile of the heating step to a temperature profile of reflow soldering (claims 1, 36), the relationship of the temperature profile of the heating step to the temperature profile of the reflow soldering step (claim 43), and the use of an outer connection terminal (claim 4) or a connection terminal (claim 43) to reflow solder the heated assembled coin- or button-type electrical double layer capacitor on the circuit substrate, claim 55 has been amended to correctly depend on claim 43, and claims 2, 5-11, 37, 39-40, 44, 46-47 and 49-54 have been canceled, thereby placing the application in condition for allowance or otherwise reducing the issues which remain for appeal.

In view of the foregoing amendments and discussion, the application is now believed to be in condition for allowance. Accordingly, entry of this amendment and favorable reconsideration and allowance of the claims are most respectfully requested.

Respectfully submitted,

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MAILING CERTIFICATE

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September 2, 2003
Date